REMARKS

This paper is responsive to the Non-Final Office Action dated March 21, 2005. Claims 1-58 were examined.

Information Disclosure Statements

Applicant filed an IDS on July 9, 2004, and an initialed copy of the Form PTO-1449 was returned in the Office action. However, one of the references was not initialed by the examiner. Applicant respectfully requests the Examiner to initial reference number AM and return another copy of Form PTO-1449 with the next Office action.

Drawings

The Office action does not indicate whether the drawings filed on September 17, 2003 are acceptable. Applicant respectfully requests the Examiner to so indicate in the next Office action.

Amendments to the Specification

Paragraph 1001 was amended to add an Application Number which was unknown at filing.

Claim Objections

Applicant has amended claim 32 as requested by the Examiner. Claim 11 has also been amended to add a colon at the end of line 1.

Claim Rejections - 35 U.S.C. § 102

Claims 1-58 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Eleyan et al. (U. S. Patent No. 6,762,961). Applicant respectfully traverses this rejection.

Eleyan et al. disclose a sensing circuit for a differential pair in a semiconductor memory which includes transistors configured in opposition and a variable delay element responsive to an accumulated data-dependent mismatch in characteristics of the opposing transistors. The variable element at least partially compensates for the characteristic mismatch by varying the

latency of a sensing operation of the sensing circuit (column 2, lines 50-56). In all the disclosed embodiments, Eleyan et al. teach adjusting the latency of the sensing operation (i.e., "adjusting the latch timing") to compensate for the mismatch that otherwise would result in errors of data read compared to data written.

Regarding claim 24, nowhere does Eleyan et al. disclose or suggest any "*preconditioning circuit* for subjecting the matched devices to a particular condition for a length of time sufficient to *cause an initial shift* in the characteristic in each of the matched devices and *to thereby reduce* an expected magnitude of *any further lifetime shift* in the characteristic of either matched device" as recited in the claim.

The Examiner has cited Eleyan et al. at column 1, lines 15-55 in support of the assertion that Eleyan et al. discloses such a preconditioning circuit. Applicant respectfully submits that this cited portion describes generally a sense amplifier and the well known relationship of an equalization signal (EQ) timing to both sensing correctness and cycle time. No circuitry other than a sense amplifier circuit, a bit line equilibration circuit, and timing circuit for strobing such a sense amplifier are even implied by such description. In particular, no such preconditioning circuit or activity is described or even implied.

In addition, the Examiner has asserted that Eleyan et al. (column 2, lines 45-48) also disclose "wherein the preconditioning circuit comprises means for applying a substantially uniform bias history across both first and second matched devices. This cited portion recites:

> In contrast, techniques, circuits, and methods described herein provide variable delay compensation for data-dependent mismatch in a characteristic of opposing devices, such as NBTI-related V_t shift based on disparate bias histories of opposing PMOS devices of a sense amplifier of a memory circuit.

Not only does this cited passage fail to describe the aforementioned means which the Examiner alleges, this passage again describes varying the delay of the sense amplifier timing to accommodate data-dependent mismatch. It suggests nothing about applying a substantially uniform bias history across both first and second matched devices. To the contrary, it specifically comprehends the precise opposite: a *data-dependent* mismatch in a characteristic of

opposing devices, such as NBTI-related V_t shift based on *disparate bias histories* of opposing PMOS devices.

Applicant respectfully traverses several of the positions advanced by the Examiner regarding subject matter allegedly disclosed by Eleyan et al. For example, the Examiner cites column 3, lines 1-30 for the proposition that Eleyan et al. teaches a preconditioning circuit "arranged to subject both matched devices simultaneously to the predetermined bias condition." Neither this cited passage, nor any other portion of Eleyan et al., describes any such circuit or related method.

As another example, the Examiner cites column 3, lines 19-30 for the proposition that Eleyan et al. teaches a preconditioning circuit which is "configured to be enabled during a burn-in operation." This cited passage mentions nothing about burn-in operations, but only mentions performing an in-situ test operation.

Regarding claims 56-58, the Examiner again alleges that Eleyan et al. discloses a preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device. Applicant respectfully traverses this position for the reasons advanced above.

Regarding the method claims 1-23, the Examiner has advanced the position that the apparatus disclosed by Eleyan et al. *would* perform the claimed method. Applicant respectfully submits that Eleyan et al. nowhere describes such a preconditioning step as recited in the claims. Even assuming, *arguendo*, that the alleged circuitry *could* perform such a preconditioning step as recited in the various claims, there nonetheless is no teaching or suggestion of doing so. Nor is such an operation inherent in such circuitry. Figure 1, as used in Eleyan et al., is described as largely conventional in design. A variable delay element is described in Fig. 3, and such a delay element used to vary the sense amplifier timing is described in Fig. 4 (which shows additional detail not present in Fig. 1).

In the instant application, Fig. 8 is described as an exemplary memory circuit which may be largely conventional in design (Page 11, Paragraph 1042), but it is specifically mentioned that the sense amplifiers are preferably implemented in accordance with the teachings of the present invention to include provisions for preconditioning matched devices (Page 12, Paragraph 1043). Such circuitry is not described in Eleyan et al. even in regards to his Fig. 1 or Fig. 4.

Summary

Claims 1-58 remain in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Andrew C. Graham — 6-21-05 Date

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Respectfully submitted,

Andrew C. Graham, Reg. No. 36,531
Attorney for Applicant(s)
(512) 338-6313 (direct)
(512) 338-6301 (fax)